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DOCUMENT 4701

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Seon Ho HAN et al

Serial No.: 10/572,901

Group Art Unit:

Filed: March 21, 2006

Examiner:

For: Voltage Controlled Digital Analog Oscillator and Frequency Synthesizer Using the Same

Certification under 37 CFR 1.8(a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with The United States Postal Service with sufficient postage as first class mail in an envelope addressed to The Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on May 23, 2006.


W. William Park, Reg. No. 55,523

The Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (IDS) WITHIN
THREE MONTHS OF FILING OR BEFORE MAILING OF FIRST OFFICE ACTION**

The information disclosure statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of the first Office Action on the merits, whichever event occurs last. 37 CFR 1.97(b).

No fee is believed to be required in view of the above. However, if this is not the case, the Commissioner is authorized to charge our Deposit Account No. 12-0400 for any required fees.

Date: May 23, 2006


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DOCKET NUMBER 4701

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INFORMATION DISCLOSURE STATEMENT (IDS)

Applicant submits herewith patents, publications or other information of which Applicant is aware, which may be material to the examination of this application and in respect of which there may be a duty to disclose under 37 CFR 1.56.

No paper copies of the U.S. patent references identified in this IDS, if any, are submitted herewith as they are no longer required by the USPTO rules. Only the copies of foreign patent and/or other relevant publication references are submitted herewith.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made (37 CFR 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability or that no other material information exists.

The filing of this information disclosure statement shall not be construed as an admission against interest in any manner. Notice of January 9, 1992, 1135 O.G. 13-25, at 25.

The references submitted herein are listed on PTO-1449 form (modified) enclosed herewith. A copy of each reference listed is being furnished except any duplicate or cumulative patents or publications specified otherwise.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AK/

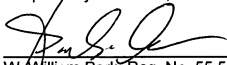
A translation of any foreign language reference, if any, is indicated in PTO-1449 form and being submitted herein if it is readily available. Otherwise it should be construed that such translation is not readily available.

Also submitted herein is a copy of the International Search Report which satisfies the requirement for a translation or concise explanation of any non-English reference cited therein, as provided in MPEP §609 A(3).

The Statement is made on the basis of the information:

X supplied by an individual associated with the filing and
prosecution of this application (37 CFR 1.56(c));
X cited in a corresponding PCT application (enclosed herein is the
International Search Report).

Respectfully submitted,



Date: May 23, 2006

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Form PTO-1049 (Modified)

FORM PTO-1449	ATTY. DOCKET NO. CU-4701	SERIAL NO. 10/572,901
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant Seon Ho HAN et al	
(37 CFR 1.98(b))	FILING DATE March 21, 2006	GROUP

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Place of publication)

/AK/		Chi-Wa Lo et al, "A 1.5-V 900-MHz Monolithic CMOS Fast-Switching Frequency Synthesizer for Wireless Applications," 2000 Symposium on VLSI Circuits Digest of Technical Papers, pp. 238-241
/AK/		Frank Herzel et al, "An Integrated CMOS PLL for Low-Jitter Applications," IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, Vol. 49, No. 6, June 2002, pp. 427-429
/AK/	Date Unknown	Tsung-Hsien Lin et al, "A 900MHz, 2.5mA CMOS Frequency Synthesizer with an Automatic SC Tuning Loop," Electrical Engineering Department, University of California, Los Angeles CA 90095-1594, pp. 375-378
/AK/		Yido Koo et al, "A Fully-Integrated CMOS Frequency Synthesizer with Charge-Averaging Charge Pump and Dual-Path Loop Filter for PCS- and Cellular-CDMA Wireless Systems," 2001 Symposium on VLSI Circuits Digest of Technical Papers, pp. 43-46
EXAMINER		DATE CONSIDERED
/Arnold Kinkead/		
EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		

(Form PTO-1449)

5-23-06

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AK/